CLAIMS

I claim:

1. A method, comprising:

depositing a graded silicon germanium layer on a substrate;

depositing a relaxed silicon germanium layer on the graded silicon germanium layer;

polishing the relaxed silicon germanium layer; and

depositing a strained silicon layer directly on the polished relaxed silicon germanium layer.

2. The method of claim 1, wherein the strained silicon layer has a first surface adjacent the polished relaxed silicon germanium layer and a second surface substantially opposite the first surface and the second surface has a roughness of about 1.0 nanometers RMS or less.

3. The method of claim 1, wherein the strained silicon layer has a first surface adjacent the polished relaxed silicon germanium layer and a second surface substantially opposite the first surface and the second surface has a roughness of about 0.5 nanometers RMS or less.

4. The method of claim 1, wherein the strained silicon layer has a thickness in a range from about 150 angstroms to about 1000 angstroms, and polishing the relaxed silicon germanium layer comprises chemical mechanically polishing the relaxed silicon germanium layer for at least approximately 60 seconds.

5. The method of claim 1, wherein depositing a relaxed silicon germanium layer comprises depositing a relaxed silicon germanium layer with a thickness in a range between about 2000 angstroms and about 5000 angstroms and polishing the relaxed silicon germanium layer comprises removing about half the thickness of the deposited relaxed silicon germanium layer.

6. The method of claim A1, wherein polishing the relaxed silicon germanium layer comprises chemical mechanically polishing the relaxed silicon germanium layer for at least approximately 60 seconds.

7. A device, comprising:

a substrate; and

a strained silicon layer on the substrate, wherein the strained silicon layer has a surface roughness of about 1.0 nanometers RMS or less.

8. The device of claim 7, further comprising a relaxed silicon germanium layer between the substrate and the strained silicon layer.

9. The device of claim 8, further comprising a graded silicon germanium layer between the substrate and the relaxed silicon germanium layer.

10. The device of claim 8, wherein the strained silicon layer is directly on the relaxed silicon germanium layer.

11. The device of claim 8, wherein relaxed silicon germanium layer has a polished surface and wherein the strained silicon layer is directly on the polished surface of the relaxed silicon germanium layer.

12. The device of claim 7, wherein the strained silicon layer has a surface roughness of about 0.5 nanometers RMS or less.

13. A device, comprising:

a substrate;

a graded silicon germanium layer on the substrate;

a relaxed silicon germanium layer on the graded silicon germanium layer, the relaxed graded silicon germanium layer having a first surface closer to the graded silicon germanium layer and a polished second surface further from the graded silicon germanium layer; and

a strained silicon layer directly on the polished second surface of the relaxed silicon germanium layer.

14. The device of claim 13, wherein the strained silicon layer has a surface roughness of about 1.0 nanometers RMS or less.

15. The device of claim 13, further comprising:

a first source/drain region adjacent the strained silicon layer;

a second source/drain region adjacent the strained silicon layer and spaced apart from the first source/drain region by the strained silicon layer; and

a gate electrode on the strained silicon layer.